What is claimed is:

1. A boot method for use in a mobile device having FLASH memory storing boot instructions and having a serial port, comprising the steps of:

reading contents of a security location in the FLASH memory;

comparing the contents of the security location to a predetermined security value; and

selectively polling the serial port for activity based on the result of the comparison.

2. A boot method according to claim 1 wherein the polling is performed if the contents of the security location do not match the predetermined security value.

3. A boot method according to claim 1 further comprising the step of jumping to a boot location in FLASH memory to execute instructions stored therein.

4. A boot method according to claim 2 further comprising the step of downloading code into internal SRAM located in the mobile device in response to a detection of serial port activity.

5. A boot method according to claim 4 further comprising the step of executing an instruction in the downloaded code.

6. A boot method according to claim 5 further comprising the step of jumping to a boot location in FLASH memory to execute boot instructions stored therein.

7. A boot method according to claim 1 wherein the predetermined security value is stored in a BootROM located in the mobile device.

8. A boot method according to claim 1 wherein the step of reading is performed in response to a reset command.

9. An apparatus for use in a mobile device having a serial port, comprising:

a first memory means having a predetermined security value stored therein;

a second memory means having a security location; and

a processor in communication with the first and second memory means for comparing the contents of the security location to the predetermined security value, and for selectively polling the serial port for activity based on the result of the comparison.

10. An apparatus according to claim 9 wherein the first memory means comprises a Boot Read Only Memory (BootROM).

11. An apparatus according to claim 9 wherein the second memory means comprises a FLASH memory.

12. An apparatus according to claim 9 further comprising a reset means in communication with the processor for initiating a reset process.

13. An apparatus according to claim 9 wherein the processor compares contents of the security location and said predetermined security value in response to initiation of a reset process.

14. An apparatus according to claim 9 wherein the first memory means is located on an ASIC.

15. An apparatus according to claim 9 wherein the processor is located on an ASIC.

16. An apparatus according to claim 9 wherein the processor comprises a microcontrol unit connected to the serial port.

17. An apparatus according to claim 9 wherein the processor comprises a digital signal processor connected to the second memory means.